CLAIMS

1. A wafer processing apparatus, comprising:

a first wafer transporter;

a first process station coupled to said first wafer transporter, said first process station including:

a first plurality of wafer processing stacks, each of said first plurality of wafer processing stacks including a first plurality of wafer processing modules, and

a second wafer transporter coupled to said first plurality of wafer processing stacks, each of said first plurality of wafer processing modules adjacent, and accessible by, said second wafer transporter;

a second process station coupled to said first wafer transporter, said second process station including:

a second plurality of wafer processing stacks, each of said second plurality of wafer processing stacks including a second plurality of wafer processing modules, and

a third wafer transporter coupled to said second plurality of wafer processing stacks, each of said second plurality of wafer processing modules adjacent, and accessible by, said third wafer transporter; and

a fourth wafer transporter coupled to both said first process station and said second process station,

wherein each of said plurality of wafer processing modules in each of said plurality of wafer processing stacks is also accessible by either said first wafer transporter or said fourth wafer transporter.

2. The wafer processing apparatus of claim 1, wherein said first plurality of wafer processing stacks and said second wafer transporter are configured to define a polygonal arrangement.

3. The wafer processing apparatus of claim 2, wherein said first plurality of wafer processing stacks and said second wafer transporter are configured to define a close pack arrangement.

4. The wafer processing apparatus of claim 3, wherein said first plurality of wafer processing stacks and said second wafer transporter are configured to define a hexagonal close pack arrangement.

5. The wafer processing apparatus of claim 1, wherein all of said first wafer transporter, said second wafer transporter, said third wafer transporter, and said fourth wafer transporter include pivotable pick and place robots, and both said second wafer transporter and said third wafer transporter are stationary with regard to lateral traverse.

6. The wafer processing apparatus of claim 5, wherein both said first wafer transporter and said fourth wafer transporter are laterally traversable.

7. The wafer processing apparatus of claim 1, further comprising an interface section coupled to said first wafer transporter, said interface section including at least one cassette station.

8. The wafer processing apparatus of claim 7, further comprising another interface section coupled to said fourth wafer transporter, said another interface section including at least one input/output port.

9. The wafer processing apparatus of claim 8, further comprising a stepper coupled to said input/output port.

10. The wafer processing apparatus of claim 1, wherein all stroke lengths defined by said first wafer transporter and said fourth wafer transporter are substantially equal.

11. The wafer processing apparatus of claim 1, wherein all stroke lengths defined by said second wafer transporter and said third wafer transporter are substantially equal.

12. The wafer processing apparatus of claim 1, wherein said first wafer transporter, said second wafer transporter, said third wafer transporter, and said fourth wafer transporter are configured to define an arrangement in which no additional wafer moves are required beyond a minimum number of wafer moves mandated by any given process flow.

13. The wafer processing apparatus of claim 1, wherein said first wafer transporter, said second wafer transporter, said third wafer transporter, and said fourth wafer transporter are configured to define an arrangement in which a total wafer transfer load is substantially equally distributed among said first wafer transporter, said second wafer transporter, said third wafer transporter, and said fourth wafer transporter.

14. The wafer processing apparatus of claim 1, wherein said first wafer transporter, said second wafer transporter, said third wafer transporter and said fourth wafer transporter all include plural wafer grippers.

15. The wafer processing apparatus of claim 1, wherein each of said plurality of wafer processing modules in each of said plurality of wafer processing stacks is bidirectionally accessible.

16. A wafer processing apparatus, comprising:

a first wafer transporter;

a process station coupled to said first wafer transporter, said process station including:

a first plurality of wafer processing stacks, each of said plurality of wafer processing stacks including a plurality of wafer processing modules, and

a second wafer transporter coupled to said plurality of wafer processing modules, each of said plurality of wafer processing modules adjacent, and accessible by, said second wafer transporter; and

a third wafer transporter coupled to said process station,

wherein any of said plurality of wafer processing modules in any of said plurality of wafer processing stacks can be accessed by at least two adjacent wafer transporters selected from the group consisting of said first wafer transporter, said second wafer transporter, and said third wafer transporter.

17. The wafer processing apparatus of claim 16, wherein said second wafer transporter transports only wafers of a single state selected from the group consisting of heated and unheated.

18. The wafer processing apparatus of claim 16, further comprising another processing station coupled to both said first wafer transporter and said third wafer transporter.

19. The wafer processing apparatus of claim 16, wherein avoidance of thermal cross-talk between wafers does not require one or more dedicated transfer arms.

20. The wafer processing apparatus of claim 16, wherein said first plurality of wafer processing stacks and said second wafer transporter are configured to define a polygonal arrangement.

21. The wafer processing apparatus of claim 20, wherein said first plurality of wafer processing stacks and said second wafer transporter are configured to define a close pack arrangement.

22. The wafer processing apparatus of claim 21, wherein said first plurality of wafer processing stacks and said second wafer transporter are configured to define a hexagonal close pack arrangement.

23. The wafer processing apparatus of claim 16, wherein all of said first wafer transporter, said second wafer transporter and said third wafer transporter include pivotable pick and place robots, and said second wafer transporter is stationary with regard to lateral traverse.

24. The wafer processing apparatus of claim 23, wherein both said first wafer transporter and said fourth wafer transporter are laterally traversable.

25. The wafer processing apparatus of claim 16, further comprising an interface section coupled to said first wafer transporter, said interface section including at least one cassette station.

26. The wafer processing apparatus of claim 25, further comprising another interface section coupled to said third wafer transporter, said another interface section including at least one input/output port.

27. The wafer processing apparatus of claim 26, further comprising a stepper coupled to said input/output port.

28. The wafer processing apparatus of claim 16, wherein all stroke lengths defined by said first wafer transporter and said third wafer transporter are substantially equal.

29. The wafer processing apparatus of claim 16, wherein said first wafer transporter, said second wafer transporter, and said third wafer transporter are configured to define an arrangement in which no additional wafer moves are required beyond a minimum number of wafer moves mandated by any given process flow.

30. The wafer processing apparatus of claim 16, wherein said first wafer transporter, said second wafer transporter, and said third wafer transporter are configured to define an arrangement in which a total wafer transfer load is substantially equally distributed among said first wafer transporter, said second wafer transporter, and said third wafer transporter.

31. The wafer processing apparatus of claim 16, wherein said first wafer transporter, said second wafer transporter and said third wafer transporter all include plural wafer grippers.

32. The wafer processing apparatus of claim 16, wherein each of said plurality of wafer processing modules in each of said plurality of wafer processing stacks is bidirectionally accessible.

33. A wafer processing apparatus, comprising:

a first wafer transporter;

a first process station coupled to said first wafer transporter, said first process station including:

a first plurality of wafer processing stacks, each of said first plurality of wafer processing stacks including a first plurality of wafer processing modules, and

a second wafer transporter coupled to said first plurality of wafer processing stacks, each of said first plurality of wafer processing modules adjacent, and accessible by, said second wafer transporter;

a second process station coupled to said first wafer transporter, said second process station including:

a second plurality of wafer processing stacks, each of said second plurality of wafer processing stacks including a second plurality of wafer processing modules, and

a third wafer transporter coupled to said plurality of wafer processing stacks, each of said second plurality of wafer processing modules adjacent, and accessible by, said third wafer transporter; and

a fourth wafer transporter coupled to both said first process station and said second process station,

wherein each of said first process station and said second process station are individually symmetrical with regard to wafer transporter access on both an X axis and a Y axis.

34. The wafer processing apparatus of claim 33, wherein said first plurality of wafer processing stacks and said second wafer transporter are configured to define a polygonal arrangement.

35. The wafer processing apparatus of claim 34, wherein said first plurality of wafer processing stacks and said second wafer transporter are configured to define a close pack arrangement.

36. The wafer processing apparatus of claim 35, wherein said first plurality of wafer processing stacks and said second wafer transporter are configured to define a hexagonal close pack arrangement.

37. The wafer processing apparatus of claim 33, wherein all of said first wafer transporter, said second wafer transporter, said third wafer transporter, and said fourth wafer transporter include pivotable pick and place robots, and both said second wafer transporter and said third wafer transporter are stationary with regard to lateral traverse.

38. The wafer processing apparatus of claim 37, wherein both said first wafer transporter and said fourth wafer transporter are laterally traversable.

39. The wafer processing apparatus of claim 33, further comprising an interface section coupled to said first wafer transporter, said interface section including at least one cassette station.

40. The wafer processing apparatus of claim 39, further comprising another interface section coupled to said fourth wafer transporter, said another interface section including at least one input/output port.

41. The wafer processing apparatus of claim 40, further comprising a stepper coupled to said input/output port.

42. The wafer processing apparatus of claim 33, wherein all stroke lengths defined by said first wafer transporter and said fourth wafer transporter are substantially equal.

43. The wafer processing apparatus of claim 33, wherein all stroke lengths defined by said second wafer transporter and said third wafer transporter are substantially equal.

44. The wafer processing apparatus of claim 33, wherein said first wafer transporter, said second wafer transporter, said third wafer transporter, and said fourth wafer transporter are configured to define an arrangement in which no additional wafer moves are required beyond a minimum number of wafer moves mandated by any given process flow.

45. The wafer processing apparatus of claim 33, wherein said first wafer transporter, said second wafer transporter, said third wafer transporter, and said fourth wafer transporter are configured to define an arrangement in which a total wafer transfer load is substantially equally distributed among said first wafer transporter, said second wafer transporter, said third wafer transporter, and said fourth wafer transporter.

46. The wafer processing apparatus of claim 33, wherein said first wafer transporter, said second wafer transporter, said third wafer transporter and said fourth wafer transporter all include plural wafer grippers.

47. The wafer processing apparatus of claim 33, wherein each of said plurality of wafer processing modules in each of said plurality of wafer processing stacks is bidirectionally accessible.